APPEAL BRIEF UNDER 37 C.F.R. § 41.37

TABLE OF CONTENTS

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Jeffrey S. Mailloux et al. Examiner: Hong Kim

Serial No.: 08/984,563 Group Art Unit: 2185

Filed: December 03, 1997 Docket: 303.623US4

For: ASYNCHRONOUSLY-ACCESSIBLE MEMORY DEVICE WITH MODE SELECTION CIRCUITRY FOR BURST OR PIPELINED OPERATION

APPEAL BRIEF UNDER 37 CFR § 41.37

Mail Stop Appeal Brief- Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This Appeal Brief is presented in support of the Notice of Appeal to the Board of Patent Appeals and Interferences, filed on November 29, 2006, from the Final Rejection of claims 59-62 and 68-69 of the above-identified Application, as set forth in the Final Office Action mailed on August 30, 2006, as well as the Advisory Action mailed on November 9, 2006.

The Commissioner of Patents and Trademarks is hereby authorized to charge Deposit Account No. 19-0743 in the amount of $500.00 which represents the requisite fee set forth in 37 C.F.R. § 41.20(b)(2). The Appellant respectfully requests consideration and reversal of the rejections of the pending claims.

1. REAL PARTY IN INTEREST

The real party in interest of the above-captioned patent application is the assignee, MICRON TECHNOLOGY, INC.

2. RELATED APPEALS AND INTERFERENCES

A first, related appeal was filed with respect to U.S. Patent Application Serial Number 08/984,561 (Atty. Ref. No. 303.623US6). However, a Notice of Allowance indicating allowance of all claims was subsequently mailed to the Appellant, and the application has now issued as U.S. Pat. No. 6,615,325. This matter never appeared before the Board.

A second, related appeal was filed with respect to U.S. Patent Application Serial Number 08/984,560 (Atty. Ref. No. 303.623US2). The Board issued a decision in this matter, allowing all claims (Appeal 2004-0414, attached hereto), and the application has now issued as U.S. Pat. No. 7,103,742. This matter is no longer before the Board.

A third, related appeal was filed with respect to U.S. Patent Application Serial Number 08/984,701 (Atty. Ref. No. 303.623US5). The Board issued a decision in this matter, allowing all claims (Appeal 2004-1705, attached hereto). The application has not yet issued, and is no longer before the Board.

A fourth, related appeal was filed with respect to U.S. Patent Application Serial Number 08/984,562 (Atty. Ref. No. 303.623US3). The Board issued a decision in this matter, allowing all claims except claim number 61 (Appeal 2005-1725, attached hereto), and the application has now issued as U.S. Pat. No. 7,124,256. This matter is no longer before the Board.

A fifth, related appeal was filed with respect to U.S. Patent Application Serial Number 08/984,560 (Atty. Ref. No. 303.623US1). However, prosecution has been reopened by the Office in this matter, and it was never pending before the Board.

There are no other appeals, interferences, or judicial proceedings known to Appellant that will have a bearing on the Board's decision in the present appeal.

3. STATUS OF THE CLAIMS

The present Application was filed on December 3, 1997 with claims 36-39. Claims 59-69, 70-74 and 75-83 were added in Amendments filed September 16, 1999, October 20, 2000 and May 1, 2001. Claims 59-62 and 68-69 stand twice rejected and are the subject of the present Appeal; claims 36-39, 63-67 and 75-83 have been allowed; claims 70-74 were previously canceled.

4. STATUS OF AMENDMENTS

An Amendment was made subsequent to the Final Office Action mailed August 30, 2006 to correct a typographical error in claim 68 and not for reasons related to patentability.

5. SUMMARY OF CLAIMED SUBJECT MATTER

This summary is presented in compliance with the requirements of Title 37 C.F.R. § 41.37(c)(1)(v), mandating a "concise explanation of the subject matter defined in each of the independent claims involved in the appeal ...". Nothing contained in this summary is intended to change the specific language of the claims described, nor is the language of this summary to be construed so as to limit the scope of the claims in any way.

Some embodiments of the invention are related to a method of accessing a memory, comprising receiving an external row address 154; choosing whether the memory is in a burst mode of operation or in a pipeline mode of operation 159; selecting a read operation or a write operation for the memory 150, 161; and executing a read or write operation in the chosen mode of operation. (Application, independent claim 59; FIGs. 9, 12; pg. 30, line 24 - pg. 33, line 21).

Some embodiments of the invention are related to a method for data transfer direction selection in a memory, comprising selecting a read or a write operation of the memory 150, 161; selecting a burst or a pipeline mode of operation for the memory 159; selecting an external address only data path 158; obtaining an external column address 151, 155; and accessing the memory when the pipeline mode of operation is selected 152, 156; and selecting an initial buffered external address data path 160; obtaining an initial external column address 162, 168; accessing the memory 165, 171; and generating internal column addresses when the burst mode of operation is selected 166, 172. (Application, independent claim 68; FIGs. 9, 12; pg. 30, line 24 - pg. 33, line 21).

Some embodiments of the invention are related to a storage device 100 comprising mode circuitry 121 configured to select between a burst mode and a pipelined mode; selection circuitry 121 for selecting between a read operation and a write operation; an external column address data path 115 for pipeline read and write operation column address retrieval; an internal column address generation module 149 for burst read and write operation column address generation; and pipelined/burst circuitry 138 coupled to the mode selection circuitry and configured to

switch between the pipelined mode and the burst mode for operating the storage device in either mode. (Application, independent claim 69; FIGs. 9-12; pg. 25, line 7 - pg. 33, line 21).

This summary does not provide an exhaustive or exclusive view of the subject matter of the Application, and the Appellant refers the reader to the appended claims and their legal equivalents for a complete statement of the various claimed embodiments.

6. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 59-62 and 68-69 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Manning (U.S. 5,610,864; hereinafter "Manning") in view of Roy (U.S. 6,065,092; hereinafter "Roy") or Ogawa (U.S. 5,293,347; hereinafter "Ogawa").

7. ARGUMENT

Claims 59-62 and 68-69 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Manning in view of Roy or Ogawa. First, the Appellant does not admit that Manning, Ogawa, or Roy are prior art, and reserves the right to swear behind these references in the future. Second, because no *prima facie* case of obviousness has been established, the Appellant respectfully traverses this rejection.

The Examiner has the burden under 35 U.S.C. § 103 to establish a *prima facie* case of obviousness. *In re Fine*, 837 F.2d 1071, 1074, 5 U.S.P.Q.2d (BNA) 1596, 1598 (Fed. Cir. 1988). The M.P.E.P. contains explicit direction to the Examiner in accordance with the *In re Fine* court:

> In order for the Examiner to establish a *prima facie* case of obviousness, three base criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *M.P.E.P.* § 2142 (citing *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d (BNA) 1438 (Fed. Cir. 1991)).

The requirement of a suggestion or motivation to combine references in a *prima facie* case of obviousness is emphasized in the Federal Circuit opinion, *In re Sang Su Lee*, 277 F.3d 1338; 61 U.S.P.Q.2D 1430 (Fed. Cir. 2002), which indicates that the motivation must be supported by evidence in the record.

No proper *prima facie* case of obviousness has been established because (1) combining the references does not teach all of the limitations set forth in the claims, (2) there is no motivation to combine the references, and (3) combining the references provides no reasonable expectation of success. Each of these points will be explained in detail, as follows.

The Combination of References Does not Teach All Limitations: As stated by the Board of Patent Appeals and interferences (BPAI), "Manning provides no details as to how the use of a pipelined structure might be accomplished. We agree with appellants. Manning's suggestion to use a pipeline architecture is insufficient to suggest switching between burst and

pipelined modes. ... Accordingly, we cannot sustain the obviousness rejection ...". BPAI, Appeal No. 2005-1725, March. 20, 2006. Thus, Manning fails to teach switching between burst and pipelined modes. This is also the case with Roy and Ogawa.

Roy describes a memory device capable of column burst activity where sequential bytes of data are accessed using a starting column and row address and a burst length. *See* Roy, Col. 26, lines 62-66. New actions may be initiated when a burst is completed. *See Id.* at Col. 27, lines 4-14. The device may also be used in a pseudo-pipelined access mode, such that a new column address is provided every cycle for a random read operation, as long as it is confined to a selected row. *See Id.* at Col. 28, lines 16-32 and Col. 33, lines 8-19. While limited access pseudo-pipelined reads may occur once per cycle, pseudo-pipelined write operations occur at only one-half the maximum channel frequency, since channel access is shared by both addresses and data. *See Id.* at Col. 33, lines 65-67. This is in direct contrast to the teachings of the Appellant, which enable true pipelined operation, with column-based switching in addition to row-based switching (*See* Application, pg. 38, lines 7-16). The Appellant was unable to find any indication that Roy teaches selecting true pipelined and burst operation "on the fly" as demonstrated by the Appellant's disclosed embodiments (indeed, such activity is not possible due to restrictions imposed by software header mode changes and channel data/address sharing that occur in Roy). For example, Roy does not permit row-based switching operation (i.e., "... cannot be used to change a row in every cycle ..."). *Id.* at Col. 38, lines 23-24.

While claims during examination should be interpreted as broadly as their terms reasonably allow, that interpretation must be tempered by the context in which the terms are used. The *Hyatt* court states that "during examination proceedings, claims are given their broadest reasonable interpretation consistent with the specification." *In re Hyatt*, 211 F.3d 1367, 1372, 54 U.S.P.Q.2D (BNA) 1664, 1667 (Fed. Cir. 2000) (emphasis added) ("During examination proceedings, claims are given their broadest reasonable interpretation consistent with the specification."; citing *In re Graves*, 69 F.3d 1147, 1152, 36 U.S.P.Q.2D (BNA) 1697, 1701 (Fed. Cir. 1995); *In re Etter*, 756 F.2d 852, 858, 225 U.S.P.Q. (BNA) 1, 5 (Fed. Cir. 1985) (en banc).).

The interpretation of the term "pipelined mode" proffered by the Office with respect to Roy is neither reasonable, nor consistent with the specification. It is not reasonable because it contradicts the meaning of the term as understood by those of skill in the art. The interpretation by the Office is also not consistent with the specification. Thus, any attempt by the Office to characterize Roy as teaching a true "pipelined mode" of operation is beyond that which should be reasonably allowed, and the rejection of claims under 35 U.S.C. § 103(a) is improper.

Ogawa presents similar difficulties, since pipelined access is described only with respect to a single mode of operation – the page mode. *See* Ogawa, Abstract and Col. 1, lines 8-12. "The page mode processing is an operation that subsequently reads out data in memory cells connected to one word line selected by a row address by sequentially changing the column address ...". Col. 4, lines 4-8. While Ogawa notes that "the present invention is not limited to the page mode, and the concept of the present invention can be similarly applied to random read/write operation" at Col. Col. 12, lines 5-10, this statement of potential use with respect to random read/write operations does not lead one of ordinary skill to understand how switching between burst and pipelined modes would be accomplished, since Ogawa does not teach any kind of switching behavior. As is the case with Roy, Ogawa provides no indication of how memory access operations can be conducted in conjunction with switching between burst an pipelined modes "on the fly" as taught by the Appellant.

Finally, as noted by the BPAI, "As indicated **supra**, we find nothing in Manning to suggest substituting a pipelined mode for the standard EDO such that selecting or switching between burst and pipelined modes can occur." BPAI, Appeal No. 2005-1725, March. 20, 2006 (emphasis in original). The Appellant also finds nothing in Manning to suggest substituting a pipelined mode for the page mode, as promoted by the Office with respect to Ogawa. Therefore, no combination of Manning and either Roy or Ogawa can provide "choosing whether the memory is in a burst mode of operation or a pipelined mode of operation" (claim 59) or "selecting a burst or a pipeline mode of operation" (claim 68), much less "mode circuitry configured to select between a burst mode and a pipelined mode" (claim 69) as claimed by the Appellant.

No Motivation to Combine the References: The Office asserts that "it would be obvious ... to include the memory selectively operable in a pipeline mode of Roy in the invention not Manning because it would increase memory performance of Manning by providing a new column address every cycle ..." However, this suggestion to combine the references overlooks the fact that neither Manning nor Roy teach switching between a pipelined mode and another mode. Neither does Ogawa.

In addition, this assertion overlooks the limitations of Roy's pseudo-pipelined access, namely: (1) read operations are confined to the same row (no row-based switching), and (2) write operations only occur at one-half the channel speed; not at the full speed of the channel.

Finally, combining Roy with Manning also overlooks the following statement in Manning: "An integrated circuit memory device is designed for high speed data access and compatibility with *existing* memory systems." (Manning, Abstract, emphasis added). The device is made to be compatible with existing systems; not radically new systems, such as that described by Roy, in which "[o]ne of the fundamental features of this architecture is the use of the same lines of a data channel for both address and control information, as well as for bi-directional data transfers. Data read and write operations within the memory device are organized into discrete "transactions," with each such transaction initiated by several sequential data words termed a "header." The header includes address and control information for a subsequent transfer of one or more bytes of data into or out of the memory device. The header can be applied to one channel for a subsequent transaction across that same channel or across another channel." *Roy*, Col. 9, lines 12-22. Thus, Manning teaches away from the asserted combination, since the two devices are fundamentally incompatible. Therefore, since there is no evidence in the record to support this assertion, as required by the *In Re Sang Su Lee* court, it appears the Examiner is actually using personal knowledge, and the Examiner is again respectfully requested to submit an affidavit supporting such knowledge as required by 37 C.F.R. § 1.104(d)(2). No such affidavit has been supplied to-date.

It is respectfully noted that the test for obviousness under § 103 must take into consideration the invention as a whole; that is, one must consider the particular problem solved by the combination of elements that define the invention. *See Interconnect Planning Corp. v.*

Feil, 774 F.2d 1132, 1143, 227 U.S.P.Q. 543, 551 (Fed. Cir. 1985) (emphasis added). References must be considered in their entirety, including parts that teach away from the claims. See MPEP § 2141.02. Since Roy teaches away from using a true pipelined mode (as well as from being used in a conventional manner), and since Ogawa teaches away from any kind of mode switching during operation, there is no motivation to combine these references.

No Reasonable Expectation of Success: Roy teaches the use of a pseudo-pipelined mode. Ogawa teaches the use of a single mode of operation, without switching. Combining either of these references with Manning would not lead one of ordinary skill in the art to expect success, since neither the function of switching, nor the design of circuitry to switch, between burst and pipelined modes would be enabled.

In summary, the references neither teach nor suggest selecting/choosing between burst and pipelined modes of operation, and the modifications suggested by the Office do not lead to a reasonable expectation of success by one of ordinary skill in the art. In fact, each of the references teach away from such a combination. Thus, the requirements of *M.P.E.P.* § 2142 have not been satisfied; and a *prima facie* case of obviousness has not been established with respect to the Appellant's claims. It is therefore respectfully requested that the rejection of claims 59-62 and 68-69 under 35 U.S.C. § 103(a) be reconsidered and withdrawn.

8. SUMMARY

For the reasons set forth above, claims 59-62 and 68-69 have not been properly rejected under 35 USC § 103(a) over any combination of Manning, Ogawa, and Roy. Reversal of the rejection and allowance of the pending claims are therefore respectfully requested. If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

JEFFREY S. MAILLOUX et al.

By their Representatives,

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Date January 25, 2007 By /Mark V. Muller/
Mark V. Muller
Reg. No. 37,509

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this ____ day of January 2007.

KATE GANNON
Name

Signature

CLAIMS APPENDIX

59. A method of accessing a memory, comprising:

receiving an external row address;

choosing whether the memory is in a burst mode of operation or in a pipeline mode of operation;

selecting a read operation or a write operation for the memory; and

executing a read or write operation in the chosen mode of operation.

60. The method of claim 59, and further comprising:

switching between the burst mode of operation and the pipelined mode of operation.

61. The method of claim 59, and further comprising:

switching between the read operation and the write operation.

62. The method of claim 59, wherein the operations are performed in a different order.

68. A method for data transfer direction selection in a memory, comprising:

selecting a read or a write operation of the memory;

selecting a burst or a pipeline mode of operation for the memory;

selecting an external address only data path, obtaining an external column address, and accessing the memory when the pipeline mode of operation is selected; and

selecting an initial buffered external address data path, obtaining an initial external column address, accessing the memory, and generating internal column addresses when the burst mode of operation is selected.

69. A storage device comprising:

mode circuitry configured to select between a burst mode and a pipelined mode;

selection circuitry for selecting between a read operation and a write operation;

an external column address data path for pipeline read and write operation column address retrieval;

an internal column address generation module for burst read and write operation column address generation; and

pipelined/burst circuitry coupled to the mode selection circuitry and configured to switch between the pipelined mode and the burst mode for operating the storage device in either mode.

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

Copies of the decisions in related appeals 2004-0414, 2004-1705, and 2005-1725 are attached.

Paper No. 37

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte JEFFEREY S. MAILLOUX,
KEVIN J. RYAN, TODD A. MERRITT,
AND BRETT L. WILLIAMS

Appeal No. 2004-0414
Application 08/984,560

ON BRIEF

Before THOMAS, BARRY and LEVY, Administrative Patent Judges.

THOMAS, Administrative Patent Judge.

DECISION ON APPEAL

Appellants have appealed to the Board from the examiner's final rejection of claims 11-21 and 59-71.

Representative claim 11 is reproduced below:

11. A storage device comprising:

control logic for selecting between a patternless addressing scheme and a patterned addressing scheme; and

switching circuitry for switching between a first pathway and a second pathway depending on which of said patternless addressing schemes and said patterned addressing scheme is selected.

The following reference is relied on by the examiner:

Manning	5,610,864	Mar. 11, 1997 (filing date Feb. 10, 1995)

Claims 11-21 and 59-71 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Manning. Appellant argues and the examiner makes reference at various portions of the answer to an inadvertent reliance upon 35 U.S.C. § 102(b) as the basis to reject the claims on appeal rather than upon 35 U.S.C. § 102(e). To expedite our consideration of the issues on this appeal, we consider the rejection in the same manner.

Rather than repeat the positions of the appellants and the examiner, reference is made to the brief and reply brief for appellants' positions, and to the answer for the examiner's positions.

OPINION

We reverse.

Each of independent claims 11, 59, 60, 61, 62, 65, 68 and 70 variously recite control logic for selecting between a patternless addressing scheme and a patterned addressing scheme

or selecting between a burst or a pipelined mode or selecting between an unpatterned pipelined and a patterned burst data pattern mode of operation. Correspondingly, each of these independent claims also requires the feature of switching circuitry which performs the switching of respective first and second pathways depending on which of the earlier recited addressing schemes is selected.

It goes without saying that those independent claims (59, 60, 61 and 70) that recite specifically selecting between a pipelined or a burst mode of operation are the most specific claims. On the other hand, the remaining independent claims (claims 11, 62, 65 and 68) more broadly recite the same features in a corresponding manner as to patternless and patterned addressing schemes. It is noted that the discussion at specification page 30 beginning at line 5 and at specification page 33 beginning at line 13 clearly indicates to the artisan that a patternless addressing scheme is only taught in the context of a pipelined mode of operation and that a patterned addressing scheme is only taught in a corresponding burst mode of operation.

With these considerations in mind, our study of Manning leads us to agree with appellant's assessment of this reference generally set forth in the paragraph bridging pages 3 and 4 of the principal brief on appeal. The examiner's position primarily relies upon Manning's Figure 1 as well as portions of columns 5-7. Column 5, lines 43-46 merely indicates that pipelined architectures exist as other types of memory architectures that may be applicable to the current disclosure in Manning, yet no details are supplied in any other portion of the reference to suggest the specific applicability of the burst mode operability of Manning's memory to a pipelined architecture, specifically as to how it would be implemented. The teachings at column 5, lines 43-62, in context, merely appear to teach the conceptual applicability of burst mode architectures to pipelined architectures but not presenting any further circuits in the remaining parts of the specification of Manning applicable to pipelined architectures.

Various modes are taught at column 6, lines 14-34 and column 7, lines 29-54 as relied upon by the examiner. These various modes, however, do not teach any switchability between a burst mode and a pipelined mode of operation as required by each of the

claims on appeal. We therefore agree with appellant's observation at the top of page 7 of the principal brief on appeal that "Manning never discusses the ability to switch or select between burst and pipelined modes of operation, or patternless and patterned addressing schemes, as claimed by the Appellants."

In order for us to sustain the examiner's rejection under 35 U.S.C. § 103, we would need to resort to speculation or unfounded assumptions to supply deficiencies in the factual basis of the rejections. In re Warner, 379 F.2d 1011, 1017, 154 USPQ 173, 178 (CCPA 1967), cert. denied, 389 U.S. 1057 (1968), reh'g denied, 390 U.S. 1000 (1968). This we decline to do.

Our reviewing court has made it clear in In re Lee, 277 F.3d 1338, 61 USPQ2d 1430 (Fed. Cir. 2002), and In re Zurko, 111 F.3d 887, 42 USPQ2d 1476 (Fed. Cir. 1997), that rejections must be supported by substantial evidence in the administrative record and that where the record is lacking in evidence, this Board cannot and should not resort to unsupported speculation. As indicated in Lee, 277 F.3d at 1343-44, 61 USPQ2d at 1433-34, the examiner's finding of whether there is a teaching, motivation or suggestion to combine the teachings of the applied references must not be resolved based on "subjective belief and unknown authority," but must be "based on objective evidence of record."

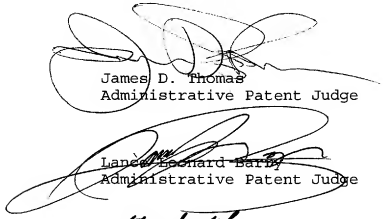
The examiner's responsive arguments portion of the answer beginning at page 5 merely repeats the initial reliance in the

statement of the rejection on certain portions of columns 5-7 of Manning. As indicated earlier, these portions of Manning clearly fall short of indicating to us the anticipatory nature of the subject matter of the claims on appeal at least as applied to pipelined memory schemes. Plainly, Manning does not explain and certainly does not show in Figure 1 of his patent switching circuitry to switch between plural pathways between a pipelined/patternless addressing scheme and a burst/patterned addressing scheme, which is the essential argument provided in the brief and reply brief by appellants. More specifically, Manning does not further develop the general statement of applicability at columns 5, lines 43-46 of his invention being usable with pipelined architectures such as to explain how a plurality of memory-type operations may occur in an overlapping manner or processed simultaneously in a manner consistent in the art and recognized to be necessary for a pipelined memory accessing scheme.

Therefore, Manning alone, within 35 U.S.C. 102(b) or § 102(e), without additional evidence, cannot be fairly said to anticipate the subject matter of each independent claim on appeal. As such, the rejection of the respective dependent claims must be reversed as well.

In view of the foregoing, the decision of the examiner rejecting all claims on appeal under 35 U.S.C. § 102 is reversed.

REVERSED



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Paper No. 42

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Ex parte JEFFREY S. MAILLOUX,
KEVIN J. RYAN,
TODD A. MERRITT
and
BRETT L. WILLIAMS

Appeal No. 2004-1705
Application 08/984,701

HEARD: February 8, 2005

Before THOMAS, BARRY and LEVY, Administrative Patent Judges.

THOMAS, Administrative Patent Judge.

DECISION ON APPEAL

Appellants have appealed to the Board from the examiner's final rejection of claims 40-43, 45, 59, 60, 62-87. At pages 2 and 4 of the answer, the examiner withdrew the rejection of claims 64, 67, 68, 73-75

and 83-85 under 35 U.S.C. § 102(a), and the separate rejection of all claims on appeal under 35 U.S.C. § 103. Only the rejection of claims 40-43, 45, 59, 60, 62, 63, 65, 66, 69-72, 76-82, 86 and 87 remain for our consideration.

Representative claim 43 is reproduced below:

43. A memory module comprising:

a plurality of memories of which at least one of said memories includes a mode select pin for switching as between a burst mode and a pipelined mode of operation.

The following reference relied on by the examiner is:

Manning	5,610,864	Mar. 11, 1997 (filing date Feb. 10, 1995)

Claims 40-43, 45, 59, 60, 62, 63, 65, 66, 69-72, 76-82, 86 and 87 stand rejected under 35 U.S.C. § 102(a) as being anticipated by Manning.

Rather than repeat the positions of the appellants and the examiner, reference is made to the brief and reply brief for the appellants' positions, and to the answer for the examiner's positions.

OPINION

We reverse.

Each of independent claims 40, 43, 59, 60, 63, 65, 66, 69, 77, 81 and 86 variously recite in some manner a mode select pin for switching between a burst mode and a pipelined mode of operation.

Our study of Manning leads us to agree with appellants' assessment of this reference generally set forth at pages 5-8 of the principal brief on appeal. The examiner's position primarily relies upon Manning's Figure 1 as well as portions of columns 5-7. Column 5, lines 43-46 merely indicates that pipelined architectures exist as other types of memory architectures that may be applicable to the current disclosure in Manning, yet no details are supplied in any other portion of the reference to suggest the specific applicability of the burst mode operability of Manning's memory to a pipelined architecture, specifically as to how it would be implemented. The teachings at column 5, lines 43-62, in context, merely appear to teach the conceptual applicability (the possibility in appellants' words) of burst mode architectures to pipelined architectures but not presenting any

further circuits in the remaining parts of the specification of Manning applicable to pipelined architectures.

Various modes are taught at column 6, lines 14-34 and column 7, lines 29-54 as relied upon by the examiner. The various modes, however, do not teach any switchability between a burst mode and a pipelined mode of operation as required by each of the claims on appeal. We therefore agree with appellants' observation at page 8 of the principal brief on appeal that "Col. 5, lines 41-50 discusses the possibility of using a pipelined architecture, but not as enabling switching between pipeline or burst operations within the same memory, as disclosed and claimed by the Appellants."

In order for us to sustain the examiner's rejection over prior art, we would need to resort to speculation or unfounded assumptions to supply deficiencies in the factual basis of the rejections. In re Warner, 379 F.2d 1011, 1017, 154 USPQ 173, 178 (CCPA 1967), cert. denied, 389 U.S. 1057 (1968), reh'g denied, 390 U.S. 1000 (1968). This we decline to do.

Our reviewing court has made it clear in In re Lee, 277 F.3d 1338, 61 USPQ2d 1430 (Fed. Cir. 2002), and In re Zurko, 111 F.3d 887, 42 USPQ2d 1476 (Fed. Cir. 1997), that rejections must be supported by substantial evidence in the administrative record and that where the record is lacking in evidence, this Board cannot and should not resort to unsupported speculation. As indicated in Lee, 277 F.3d at 1343-44, 61 USPQ2d at 1433-34, the examiner's positions must not be resolved based on "subjective belief and unknown authority," but must be "based on objective evidence of record."

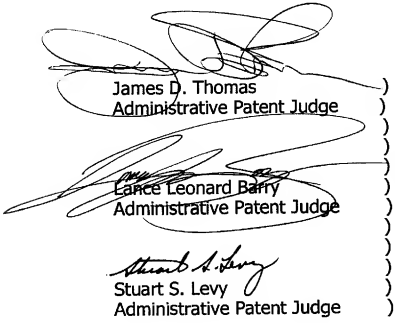
The examiner's responsive arguments portion of the answer beginning at the fourth page merely repeats the initial reliance in the statement of the rejection on certain portions of columns 5-7 of Manning. As indicated earlier, these portions of Manning clearly fall short of indicating to us the anticipatory nature of the subject matter of the claims on appeal at least as applied to pipelined memory schemes. Plainly, Manning does not explain and certainly does not show in Figure 1 of his patent switching circuitry to switch between a pipelined mode addressing

scheme and a burst mode addressing scheme, which is the essential argument provided in the brief and reply brief by appellants. More specifically, Manning does not further develop the general statement of applicability at column 5, lines 43-46 of his invention being usable with pipelined architectures such as to explain how a plurality of memory-type operations may occur in an overlapping manner or processed simultaneously in a manner consistent in the art and recognized to be necessary for a pipelined memory accessing scheme.

Therefore, Manning alone, within 35 U.S.C. § 102(a), without additional evidence, cannot be fairly said to anticipate the subject matter of each independent claim on appeal. As such, the rejection of the respective dependent claims must be reversed as well.

In view of the foregoing, the decision of the examiner rejecting all claims on appeal under 35 U.S.C. 102 is reversed.

REVERSED



James D. Thomas
Administrative Patent Judge)
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) BOARD OF PATENT
Lance Leonard Barry) APPEALS AND
Administrative Patent Judge) INTERFERENCES
)
)
)
Stuart S. Levy)
Administrative Patent Judge)

JDT/cam

Appeal No. 2004-1705
Application No. 08/984,701

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte JEFFREY S. MAILLOUX, KEVIN J. RYAN, TODD A. MERRITT, and BRETT L. WILLIAMS

Appeal No. 2005-1725
Application No. 08/984,562

HEARD: October 19, 2005

Before DIXON, GROSS, and BLANKENSHIP, ***Administrative Patent Judges***.
GROSS, ***Administrative Patent Judge***.

DECISION ON APPEAL

This is a decision on appeal from the examiner's final rejection of claims 22 through 32, 59, 61, 63, and 66 through 72, which are all of the claims pending in this application.

Appellants' invention relates to a memory device that selectively operates in either burst or pipelined modes. Claim 22 is illustrative of the claimed invention, and it reads as follows:

22. A memory circuit, comprising:

control logic for providing a selected mode control signal;

selection and temporary storage circuitry for receiving and storing a first external address; and

a multiplexer coupled to the selection and temporary storage circuitry and to the control logic for receiving the first external address and the selected mode control signal respectively therefrom and for switching the memory circuit between a burst mode and a pipelined mode.

The prior art references of record relied upon by the examiner in rejecting the appealed claims are:

Manning	5,610,864	Mar. 11, 1997 (Filed Feb. 10, 1995)
Manning (Manning II)	5,729,503	Mar. 17, 1998 (Filed Jul. 24, 1995)

Claims 22 through 32, 59, 61, and 66 through 72 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Manning.

Claims 22 through 32, 59, 61, 63, and 66 through 72 stand rejected under 35 U.S.C. § 103 as being unpatentable over Manning II in view of Manning.

Reference is made to the Final Rejection (Paper No. 29, mailed October 23, 2002), the Examiner's Answer (Paper No. 32, mailed June 3, 2003), and the Supplemental Examiner's Answer (Paper No. 37, mailed February 23, 2004) for the examiner's complete reasoning in support of the rejections, and to appellants' Brief (Paper No. 31, filed February 10, 2003), Reply Brief (Paper No. 34, filed August 7, 2003), and Supplemental

Reply Brief (Paper No. 39, filed March 26, 2004) for appellants' arguments thereagainst.

OPINION

We have carefully considered the claims, the applied prior art references, and the respective positions articulated by appellants and the examiner. As a consequence of our review, we will reverse the anticipation rejection of claims 22 through 32, 59, and 66 through 72 but affirm the anticipation rejection of claim 61. Likewise, we will reverse the obviousness rejection of claims 22 through 32, 59, 63, and 66 through 72 but affirm the obviousness rejection of claim 61.

Regarding the anticipation rejection of independent claims 22, 59, and 66, the examiner (Answer, pages 8 and 10) directs attention to column 6, lines 14-16, and column 7, lines 44-55, for the claimed switching between a burst mode and another mode and to column 5, lines 43-49, for the claimed pipelined mode. The examiner reasons (Answer, pages 8 and 10) that "in order to work in a standard EDO memory including a pipeline architecture, one has to select a pipelined mode if one is in a burst mode." The examiner continues with an explanation as to why it would

have been obvious to include a pipelined architecture in the system of Manning.

Appellants contend (Brief, page 9) that although Manning mentions the possibility of using a pipelined architecture, and discloses switching between burst and standard EDO modes, Manning fails to disclose selecting or switching between burst and pipelined modes of operation. We agree. Manning merely teaches that there may be a pipelined mode or there may be switching between two modes, one of which may be a burst mode. We find nothing in Manning to suggest that the standard EDO mode is, or could be, a pipelined mode of operation. Accordingly, we cannot sustain the anticipation rejection of claims 22, 59, and 66, nor of their dependents, claims 23 through 32 and 67 through 72.

Claim 61 does not require switching or selecting between burst and pipeline modes. Instead, the switching in claim 61 is merely between two modes of operation, which could include Manning's burst and standard EDO modes. However, claim 61 also recites that control logic provides "an internal mode control signal." Appellants' sole argument for claim 61 (Brief, pages 7 and 8) is that Manning only uses an external mode control signal. However, appellants fail to point to anything in the reference that would suggest an external mode control signal rather than an

internal mode control signal. Attorney argument cannot take the place of evidence in the record. ***Estee Lauder Inc. v. L'Oreal, S.A.***, 129 F.3d 588, 595, 44 USPQ2d 1610, 1615 (Fed. Cir. 1997). Therefore, we find appellants' argument unpersuasive, and we will affirm the anticipation rejection of claim 61 over Manning.

For the obviousness rejection of claims 22 through 32, 59, and 66 through 72, the examiner applies Manning II in view of Manning. The examiner acknowledges (Final Rejection, pages 6-7) that Manning II discloses switching between a burst mode and a page mode rather than between a burst mode and a pipelined mode, as recited in independent claims 22, 59, and 66. In fact, Manning II fails to disclose a pipelined mode at all. The examiner, however, asserts (Final Rejection, page 7) that

> it was well known in the memory art . . . to use the pipeline mode to access memory per each cycle thereby increasing the access speed. For example, Manning (864) discloses a pipelined mode (col. 5 lines 43-50) for he [sic] purpose of increasing the throughput by accessing data per every cycle (col 5 lines 46-48) thereby increasing the system throughput.

The examiner concludes that it would have been obvious to "modify a page mode of 503 with a pipelined mode of 864 because it would increase the throughput by accessing data per every cycle thereby increasing the system throughput."

Appellants argue (Brief, page 10) that Manning fails to disclose switching between burst and pipelined modes. Although Manning discusses the possibility of using a pipelined structure, appellants explain (Brief, page 10), Manning provides no details as to how the use of a pipelined structure might be accomplished. We agree with appellants. Manning's suggestion to use a pipelined structure is insufficient to suggest switching between burst and pipelined modes. As indicated ***supra***, we find nothing in Manning to suggest substituting a pipelined mode for the standard EDO such that selecting or switching between burst and pipelined modes can occur. Accordingly, we cannot sustain the obviousness rejection of claims 22, 59, and 66, nor of their dependents, claims 23 through 32 and 67 through 72.

Regarding claim 63, the "wherein" clause at the end of the claim appears to be incorrect. We believe that the claim should end with "when the selected mode control signal indicates a ***burst*** mode" (emphasis ours). We are treating this as an obvious informality that was acknowledged at the oral hearing on October 19, 2005. As such, claim 63 recites that the mode control signal selects either a pipeline mode or a burst mode. As we indicated ***supra***, we find no disclosure in either Manning or Manning II to

suggest selecting between burst and pipelined modes of operation. Accordingly, we cannot sustain the rejection of claim 63.

As to claim 61, appellants' sole argument (Brief, pages 13 and 16) is that neither Manning nor Manning II discloses an internal mode control signal without pointing to any evidence supporting appellants' assertion. Without any supporting evidence, appellants' assertion is insufficient to overcome the prima facie case of obviousness presented by the examiner. Accordingly, we will affirm the obviousness rejection of claim 61.

CONCLUSION

The decision of the examiner rejecting claims 22 through 32, 59, and 66 through 72 under 35 U.S.C. § 102 and claims 22 through 32, 59, 63, and 66 through 72 under 35 U.S.C. § 103 is reversed. However, the decision of the examiner rejecting claim 61 under 35 U.S.C. §§ 102 and 103 is affirmed. Accordingly, the examiner's decision is affirmed-in-part.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § § 1.136(a)(1)(iv).

AFFIRMED-IN-PART

JOSEPH L. DIXON)
Administrative Patent Judge)
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ANITA PELLMAN GROSS) BOARD OF PATENT
Administrative Patent Judge) APPEALS
) AND
) INTERFERENCES
)
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HOWARD B. BLANKENSHIP)
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Appeal No. 2005-1725
Application No. 08/984,562

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